Features

- Dual channel level shift and repeater for SDA/SCL Lines in I2C Applications and SMBus Compatible
- Support multi-mode: Standard-mode (SM), Fast-mode (FM), and Fast-mode Plus (FM+)
- Open-Drain I^2C Input/Output
- Allows Voltage-Level Translation Between
  - V_{REF1} range 0.8V to 5.5V
  - V_{REF2} range 2.2V to 5.5V
- 5 V tolerant I^2C-bus and enable pins
- High-impedance SCL1, SDA1, SCL2 and SDA2 pins for EN = LOW
- Support Low level output current up to 30mA
- Latch-Up performance exceeds 600mA
- ESD Protection:
  - 7000-V Human-Body Model
  - 1500-V Charged-Device Model

Description

The TPT29617A device is a dual channel I^2C level shift and repeater function with an enable (EN) input, and work from 0.8V to 5.5V V_{REF1} and 2.2V to 5.5V V_{REF2}.

The SCL1 and SDA1 I/O are connected to the SCL2 and SDA2 I/O, will allow bidirectional data flow between ports. If EN is low, the translator switch is off, and a high-impedance state exists between ports to isolate both sides.

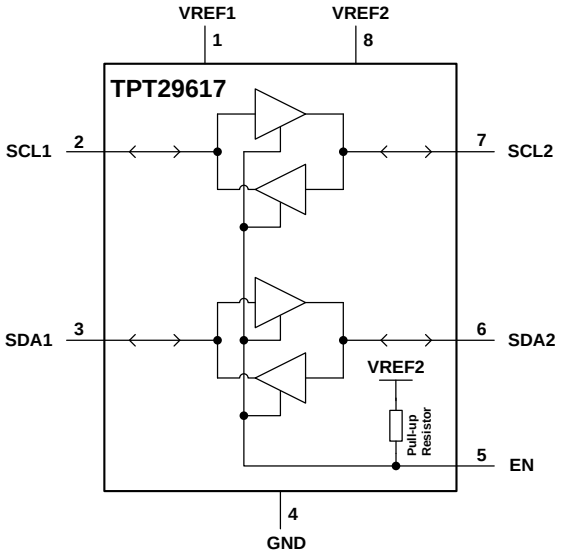
2 channel, bidirectional buffer isolates capacitance and allows 540 pF on either side of the device at 1 MHz and up to 4000 pF at lower speeds.

TPT29617A is available in SOP8 and MSOP8 package, and is characterized from –40°C to +125°C.

Applications

- I2C, SMBus, PMBus, MDIO, UART, Low-Speed SDIO, GPIO, and Other Two-Signal Interfaces
- Servers/Storages
- Routers (Telecom Switching Equipment)
- Personal Computers/Consumer handsets
- Industrial Automation

Function block



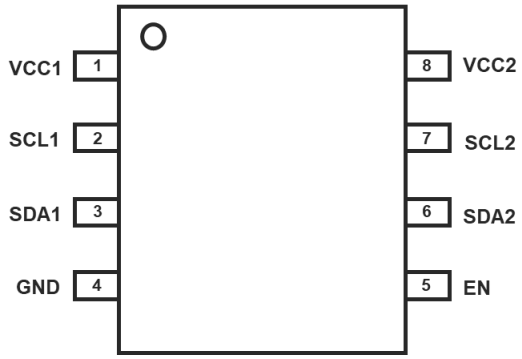
Revision History

Date	Revision	Notes
2019/6/10	Rev. Pre 0.1	Initial Version
2019/9/12	Rev. Pre 0.2	Add ESD data
2019/12/4	Rev. Pre 0.3	Add electrical data
2020/1/10	Rev. Pre 0.4	Update function block diagram and application circuit
2020/2/27	Rev. 0	Fix datasheet
2020/4/24	Rev. A	Update latch up 600mA
2020/7/21	Rev. B	Update V_{OL}-V_{IL} value

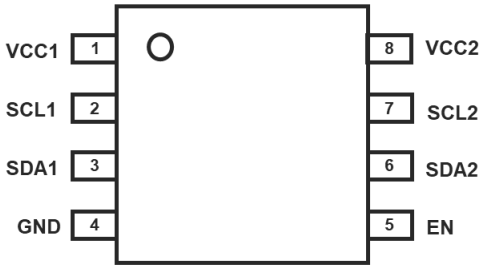
Table of Contents

Pin Configuration and Functions

TPT29617A-SO1R
SOP8



TPT29617A-VS1R
MSOP8



Pin Functions

Pin name	Pin No	I/O	Description
VREF1	1	I	side-1 supply voltage (0.8 V to 5.5 V)
SCL1	2	I/O	I^2C SCL line, side-1. Connect to VREF1 through a pull-up resistor.
SDA1	3	I/O	I^2C SDA line, side-1. Connect to VREF1 through a pull-up resistor.
GND	4	I	Supply ground
EN	5	I	Active-high repeater enable input, internal pull high to VREF2
SDA2	6	I/O	I^2C SDA line, side-2. Connect to VREF2 through a pull-up resistor.
SCL2	7	I/O	I^2C SCL line, side-2. Connect to VREF2 through a pull-up resistor.
VREF2	8	I	side-2 and device supply voltage (2.2 V to 5.5 V)

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity
TPT29617A-VS1R	-40 to 125°C	8-Pin MSOP	9617A	MSL3	Tape and Reel, 3000
TPT29617A-SO1R	-40 to 125°C	8-Pin SOP	9617A	MSL3	Tape and Reel, 4000

Absolute Maximum Ratings

Parameter		Min	Max	Unit
V_{REF1}	DC reference voltage range	–0.5	7	V
V_{REF2}	DC reference bias voltage range	–0.5	7	V
V_I	Input voltage range	–0.5	7	V
$V_{I/O}$	Input/output voltage range	–0.5	7	V
I_{IK}	Input clamp current $V_I < 0$		-50	mA
I_{OK}	Output clamp current $V_{I/O} < 0$		-50	mA
$T_{j(max)}$	Maximum junction temperature		150	°C
T_{stg}	Storage temperature range	–65	150	°C

* Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(1) This data was taken with the JEDEC low effective thermal conductivity test board.
(2) This data was taken with the JEDEC standard multilayer test boards.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001	7	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002	1.5	kV

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
MSOP8	180	72	°C/W
SOP8	148	48	°C/W

Recommended Operating Conditions

Symbol	Description	MIN	MAX	UNIT
$V_{I/O}$	Input/output voltage SCL1, SDA1, SCL2, SDA2	0	5.5	V
V_{REF1} (1)	Reference voltage	0.8	5.5	V
V_{REF2} (1)	Reference voltage	2.2	5.5	V
Iinput	Input clamp current	0	50	mA
Ioutput	Output clamp current	0	50	mA
T_A	Operating ambient temperature	–40	125	°C

Electrical Characteristics

VREF1 = 0.8 V to 5.5 V, VREF2 = 2.2 V to 5.5 V, GND = 0 V, TA = –40°C to 125°C (unless otherwise noted)

	Parameter		Test Conditions	V_{CCx}	Min	Typ	Max	Unit
V_{IK}	Input clamp voltage		I_I = –18 mA	2.2 V to 5.5 V	-1.2		–0.3	V
V_{OL}	Low-level output voltage	SDA1, SCL1	I_{OL} = 13mA	0.8 V to 5.5 V		0.1	0.2	V
		SDA2, SCL2	I_{OL} =150uA or 13mA, V_{ILA} = 0 V	2.2 V to 5.5 V		0.5	0.6	
V_{IH}	High-level input voltage	SDA1, SCL1		0.8 V to 5.5 V	0.7VREF1		5.5	V
		SDA2, SCL2		2.2 V to 5.5 V	0.7VREF2		5.5	
		EN		2.2 V to 5.5 V	0.7VREF2		5.5	
V_{IL}	Low-level input voltage	SDA1, SCL1		0.8 V to 5.5 V			0.3VREF1	V
		SDA2, SCL2		2.2 V to 5.5 V			0.4	
		EN		2.2 V to 5.5 V			0.3VREF2	
V_{OL}-V_{IL}	Difference between Low-level output and Low-level input voltage		V_{OL} at I_{OL} = 1 mA;			90	140	mV
I_{CC1}	Quiescent supply current for VREF1		Both channels low, SDA1 = SCL1 = GND and SDA2 = SCL2 = open, or	VREF1=0.8 V		1.5	5	µA
			SDA1 = SCL1 = open and SDA2 = SCL2 = GND	VREF1=5.5 V		10	20	
I_{CC2}	Quiescent supply current		Output Low Level	2.2 V to 5.5 V		9	15	mA
			Output High Level			1.2	5	
I_I	Input leakage current	SDA2, SCL2	V_I = VREF2	2.2 V to 5.5 V	–1		+1	µA
			V_I = 0.2 V, EN = 0		–1		+1	
		SDA1, SCL1	V_I = VREF1		–1		+1	
			V_I = 0.2 V		–1		+1	
		EN	V_I = VREF2		–1		+1	
			V_I = 0.2 V		–18	-7		
C_I	Input capacitance (1)	SCL1, SCL2	V_I = 3 V or 0 V	3.3 V or 0V		7		pF
		EN	V_I = 3 V or 0 V	3.3 V		5		
C_{IO}	Input/output capacitance (1)	SDA1, SDA2	V_I = 3 V or 0 V	3.3 V		10		pF

Note

(1): Test data based on bench test and design simulation

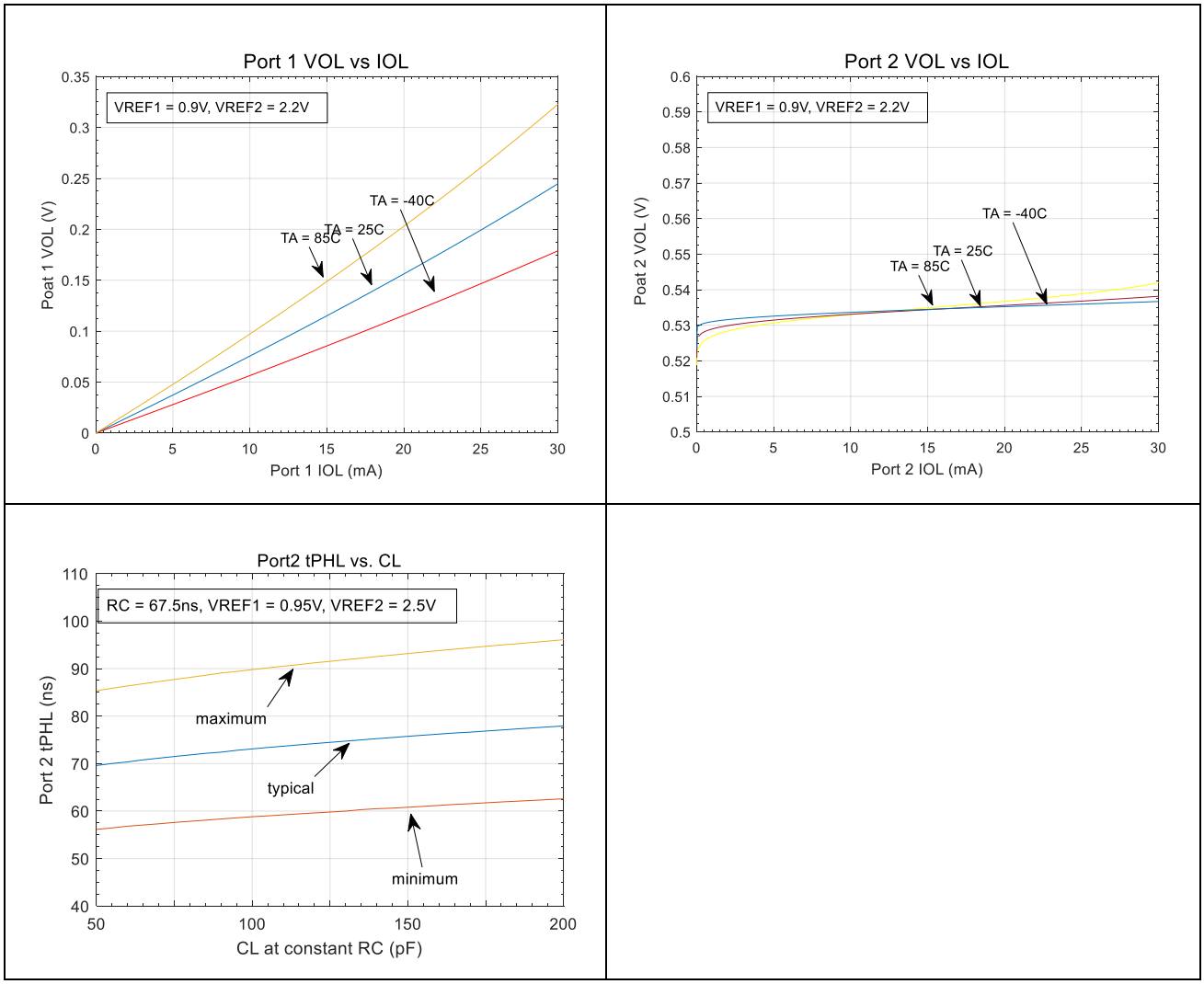
AC Timing Requirements

VREF1 = 0.8 V to 5.5 V, VREF2 = 2.2 V to 5.5 V, GND = 0V, TA = –40°C to 125° (unless otherwise noted)

Parameter			From (Input)	To (Output)	Test Conditions	Min	Typ	Max	Unit
t_{PLH}	Propagation delay		SDA2, SCL2	SDA1, SCL1			80	150	ns
			SDA1, SCL1	SDA2, SCL2	VREF2 = 2.2 to 5.5 V		85	150	ns
t_{PHL}	Propagation delay		SDA2, SCL2	SDA1, SCL1			55	100	ns
			SDA1, SCL1	SDA2, SCL2			90	150	ns
t_{TLH}	Transition time	2 side	30% Level	70% Level			90	150	ns
		1 side					75	100	ns
t_{THL}	Transition time	2 side	70% Level	30% Level			10	30	ns
		1 side					10	30	
t_{en}	Setup time, EN high before Start condition							100	ns
t_{dis}	Disable time							100	ns

Typical Performance characteristics:

VREF1 = 0.9V, VREF2 = 2.2V



Parameter measurement waveforms:

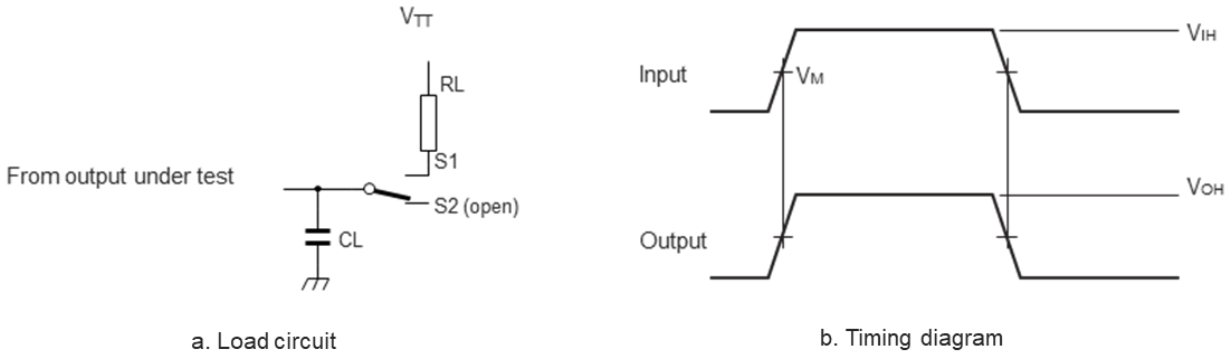


Figure 1. Load circuit for outputs

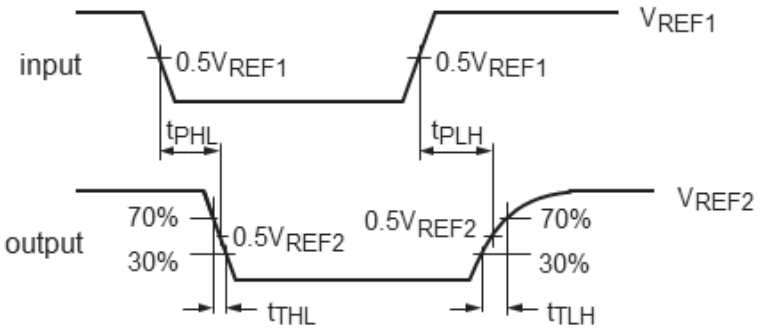


Figure 2. Propagation delay and transition times, side1 to side2

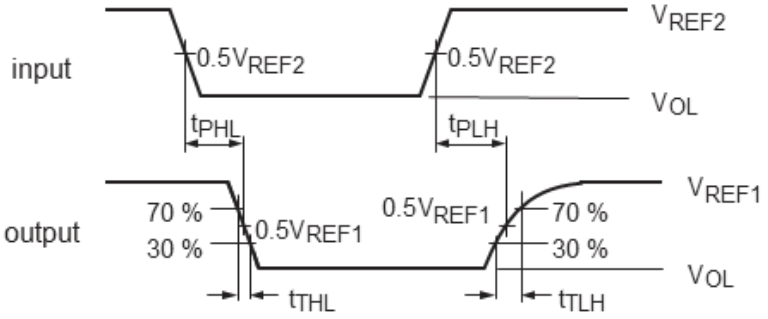


Figure 3. Propagation delay and transition times, side2 to side1

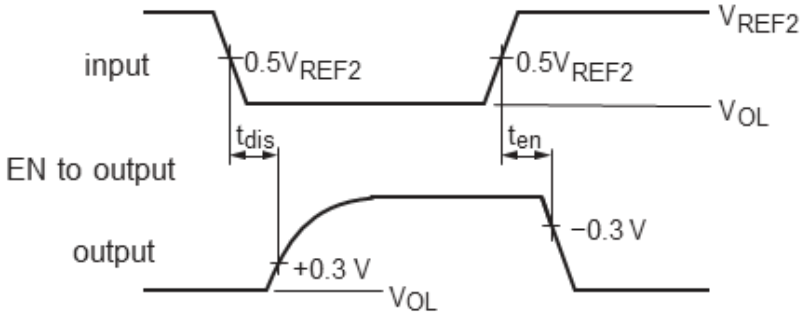
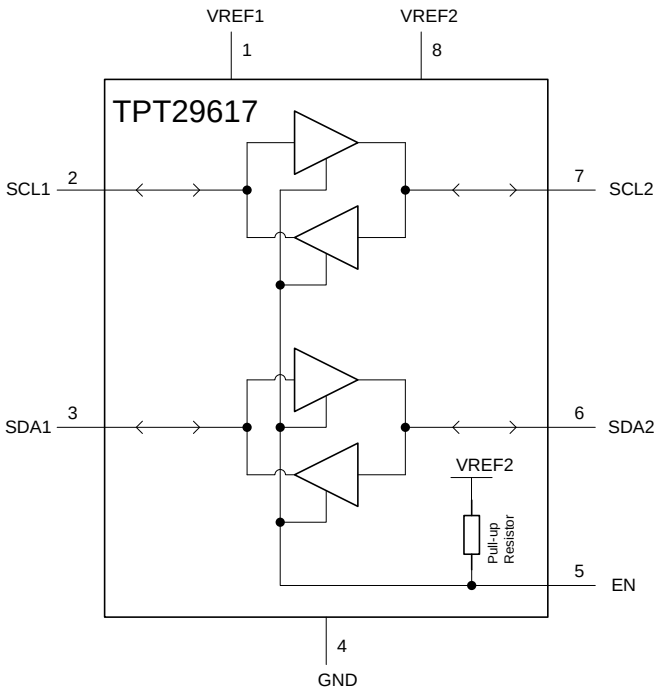


Figure 4. Enable and disable times

Function Block diagram:



Theory of Operation

General description

The TPT29617A is a dual channel level shift and repeater for SDA/SCL Lines in I2C Applications and SMBus Compatible, which supports I2C-bus or SMBus translation down to VREF1 as 0.8 V with normal system performance. The TPT29617A build in two bidirectional open-drain buffers specifically designed to support up-translation/down-translation between the low voltage (down to 0.8 V) and a 2.5 V, 3.3 V or 5 V I2C-bus or SMBus, and all inputs and I/Os are tolerant to 5.5 V level. The TPT29617A includes a power-up circuit that keeps the output drivers turned off until VREF2 is above 2.2 V and until after the internal reference circuits have settled ~400 us, and the VREF1 is above 0.8 V. VREF2 and VREF1 can be applied in any sequence at power-up. After power-up and with the enable (EN) HIGH, a LOW level on port-1 (<0.3*VREF1) turns the corresponding port-2 driver (SDA or SCL) on and drives port-2 down to ~0.55 V. When port-1 rises above 0.3*VREF1, the port-2 pull-down driver is turned off and the external pull-up resistor pulls the pin HIGH. When port-2 falls first and goes below 0.4 V, the port-1 driver is turned on and port-1 pulls down to ~0 V. The port-1 pull-down is not enabled unless the port-2 voltage goes below 0.4 V. If the port-2 low voltage goes below 0.4 V, the port-2 pull-down driver is enabled and port-2 will only be able to rise to 0.55 V until port-1 rises above 0.3*VREF1, then port-2 will continue to rise being pulled up by the external pull-up resistor. The VREF1 is only used to provide the 0.35*VREF1 reference to the port-1 input comparators and for the power good detect circuit. The TPT29617A includes a VREF1 overvoltage disable that turns the channel off if 0.4*VREF1 + 0.8 V > VREF2.

Enable (EN)

The EN pin is active HIGH with thresholds referenced to VREF2 and an internal pull-up to VREF2 that maintains the device active unless the user selects to disable the TPT29617A to isolate a badly behaved slave on power-up until after the system power-up reset. It should never change state during an I2C-bus operation because disabling during a bus operation will hang the bus and enabling part way through a bus cycle could confuse the I2C-bus parts being enabled. The enable does not switch the internal reference circuits so the ~400 us delay is only seen when VREF2 comes up.

The EN pin should only change state when the global bus and the repeater port are in an idle state to prevent system failures.

Device Function table

Input EN(1)	Translator Function
H	SCL1 = SCL2, SDA1 = SDA2
L	Disconnect

(1) The SCL switch conducts if EN is ≥ 1 V higher than SCL1 or SCL2. The same is true of SDA.

(2) EN=Floating, or the GPIO goes Hi-z which control the EN from I2C master, and TPT29617A status refer to EN=H

I2C-bus systems

As the standard I2C-bus system, pull-up resistors are required to provide the logic HIGH levels on the buffered bus (standard open-collector configuration of the I2C-bus). The size of these pull-up resistors depends on the system, but each side of the repeater must have a pull-up resistor. This part designed to work with Standard mode, Fast-mode and Fast-mode Plus I2C-bus devices in addition to SMBus devices. Standard mode and Fast-mode I2C-bus devices only specify 3 mA output drive; this limits the termination current to 3 mA in a generic I2C-bus system where Standard-mode devices, Fast-mode devices and multiple masters are possible. When only Fast-mode Plus devices are used with 20 mA at 5 V drive strength, then lower value pull-up resistors can be used. The side-2 RC should not be less than 67.5 ns because shorter RCs increase the turnaround bounce when the side-2 transitions from being externally driven to pulled down by its offset buffer.

Please see Application information, the pull up resistors value, which contains typical, star network and series network circuits.

Application information

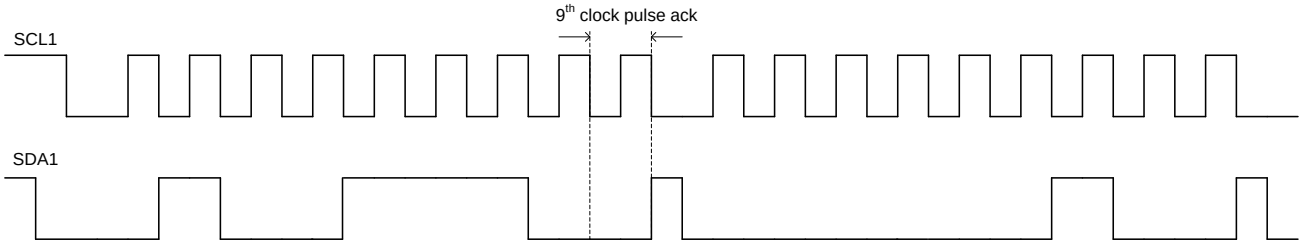


Figure 5. BUS-1（0.8V~5.5V) waveform

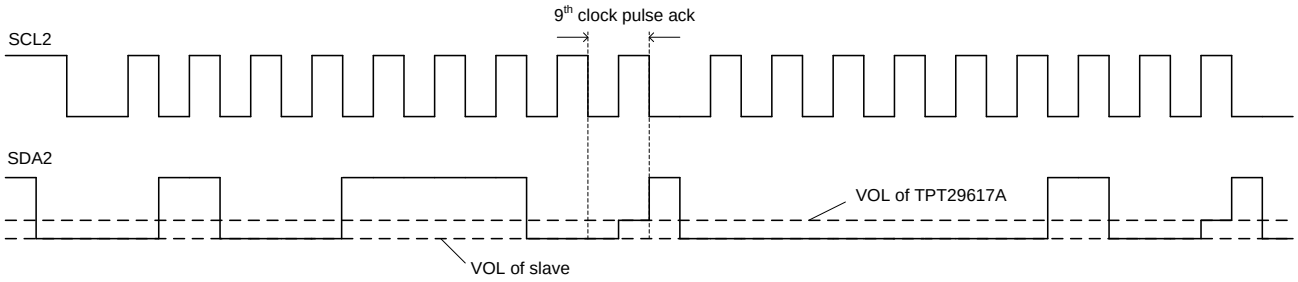


Figure 6. BUS-2 (2.2V~5.5V) waveform

A typical application is shown in Figure 7. In this example, the system master is running on a 1.8 V I2C-bus while the slave is connected to a 3.3 V bus. Both buses run at 1000 kHz. Master devices can be placed on either bus.

The TPT29617A is 5 V tolerant, so it does not require any additional circuitry to translate between 0.8 V to 5.5 V bus voltages and 2.2 V to 5.5 V bus voltages.

When port-1 of the TPT29617A is pulled LOW by a driver on the I2C-bus, a comparator detects the falling edge when it goes below 0.3*VCC(A) and causes the internal driver on port-2 to turn on, causing port-2 to pull down to about 0.5 V. When port-2 of the TPT29617A falls, first a CMOS hysteresis type input detects the falling edge and causes the internal driver on port-1 to turn on and pull the port-1 pin down to ground. In order to illustrate what would be seen in a typical application, refer to Figure 5 and Figure 6. If the bus master in Figure 7 were to write to the slave through the TPT29617A, waveforms shown in Figure 5 would be observed on the bus-1. This looks like a normal I2C-bus transmission except that the HIGH level may be as low as 0.8 V, and the turn on and turn off of the acknowledge signals are slightly delayed.

The internal comparator requires that 0.4*VREF1 be less than or equal to VREF2 - 0.8 V for the device to operate. Since A port is 5 V tolerant, the VREF1 can be lowered to support device spectrum while still supporting 5 V signals on the port-1.

On the bus-2 side of the TPT29617A, the clock and data lines would have a positive offset from ground equal to the VOL of the TPT29617A. After the eighth clock pulse, the data line will be pulled to the VOL of the slave device which is very close to ground in this example. At the end of the acknowledge, the level rises only to the LOW level set by the driver in the

TPT29617A for a short delay while the bus-1 side rises above 0.3*VCC(A) then it continues HIGH. It is important to note that any arbitration or clock stretching events require that the LOW level on the B bus side at the input of the TPT29617A (VIL) be at or below 0.4 V to be recognized by the TPT29617A and then transmitted to the bus-1 side.

Multiple TPT29617A port-1 sides can be connected in a star configuration (Figure 8), allowing all nodes to communicate with each other.

Multiple TPT29617As can be connected in series (Figure 9) as long as port-1 is connected to port-2. I2C-bus slave devices can be connected to any of the bus segments. The number of devices that can be connected in series is limited by repeater delay/time-of-flight considerations on the maximum bus speed requirements.

Decoupling capacitors not shown for simplicity, but they are required. It is especially important that the decoupling for the TPT29617A VREF2 be close to the VREF2 pin.

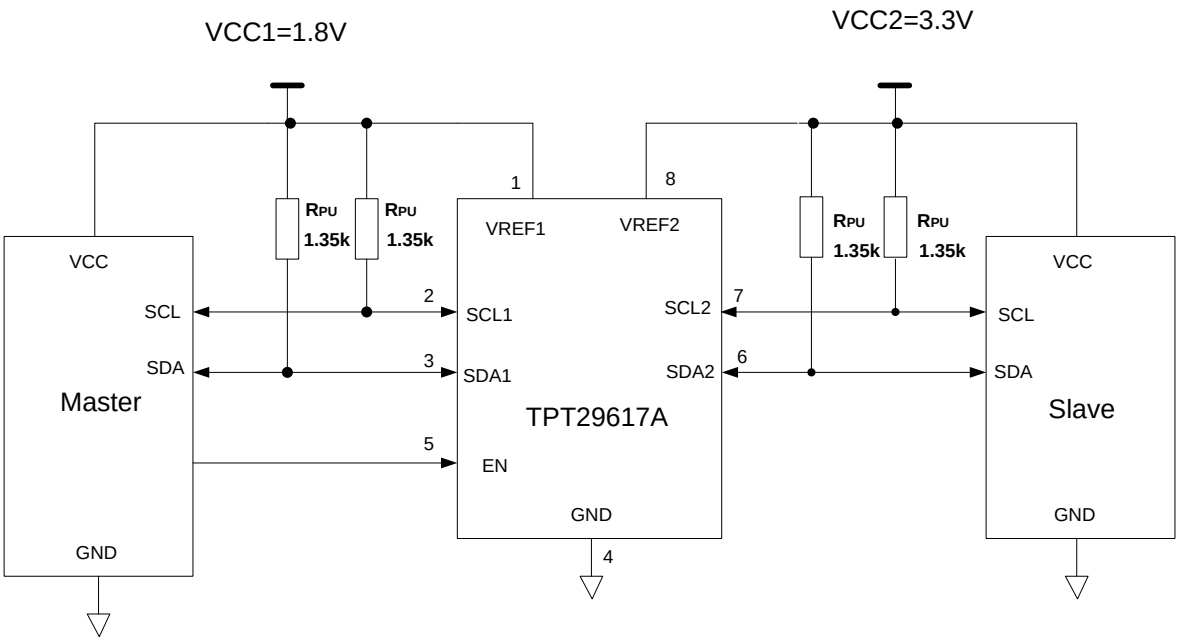


Figure 7. Typical application circuit

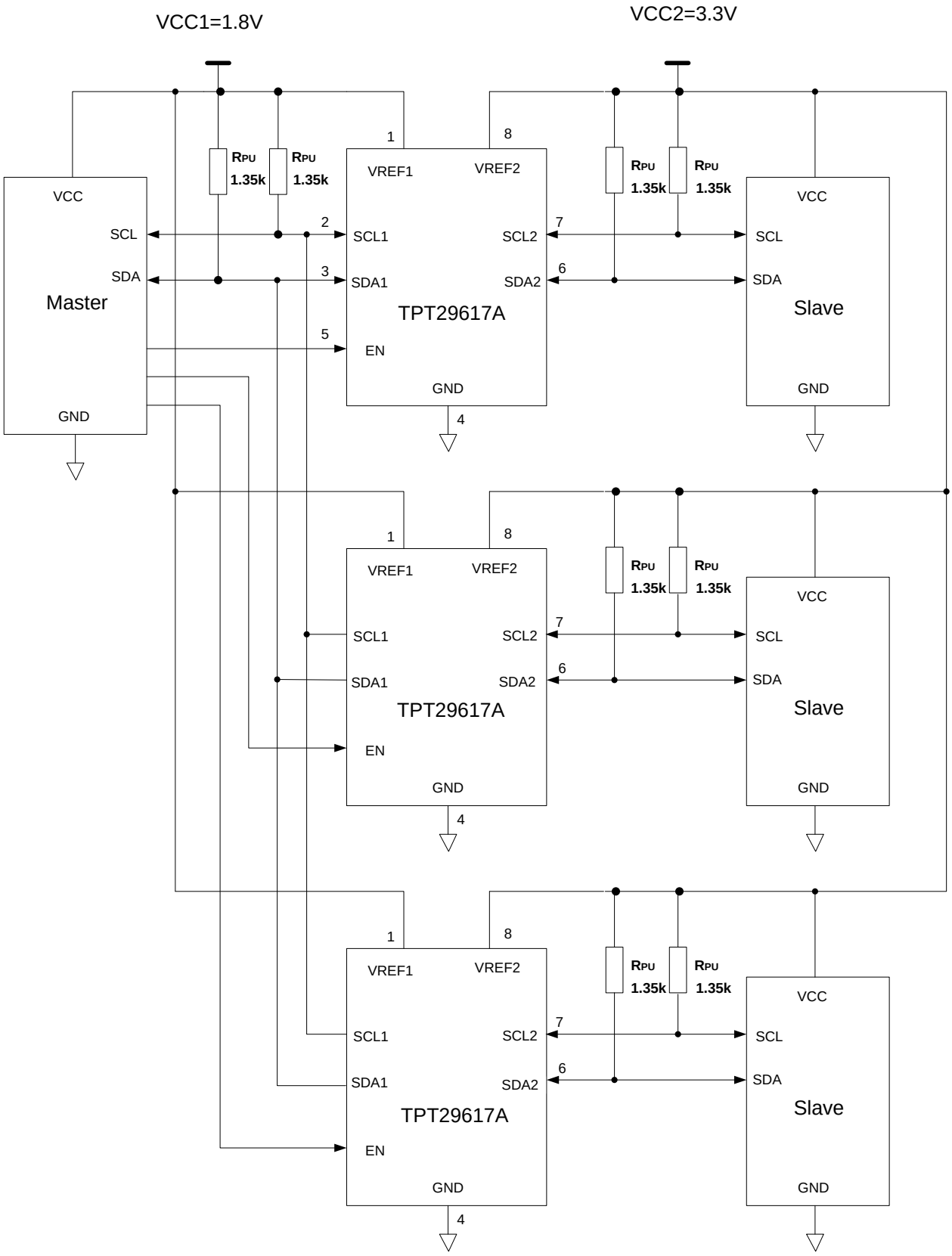


Figure 8. Typical application circuit, star network

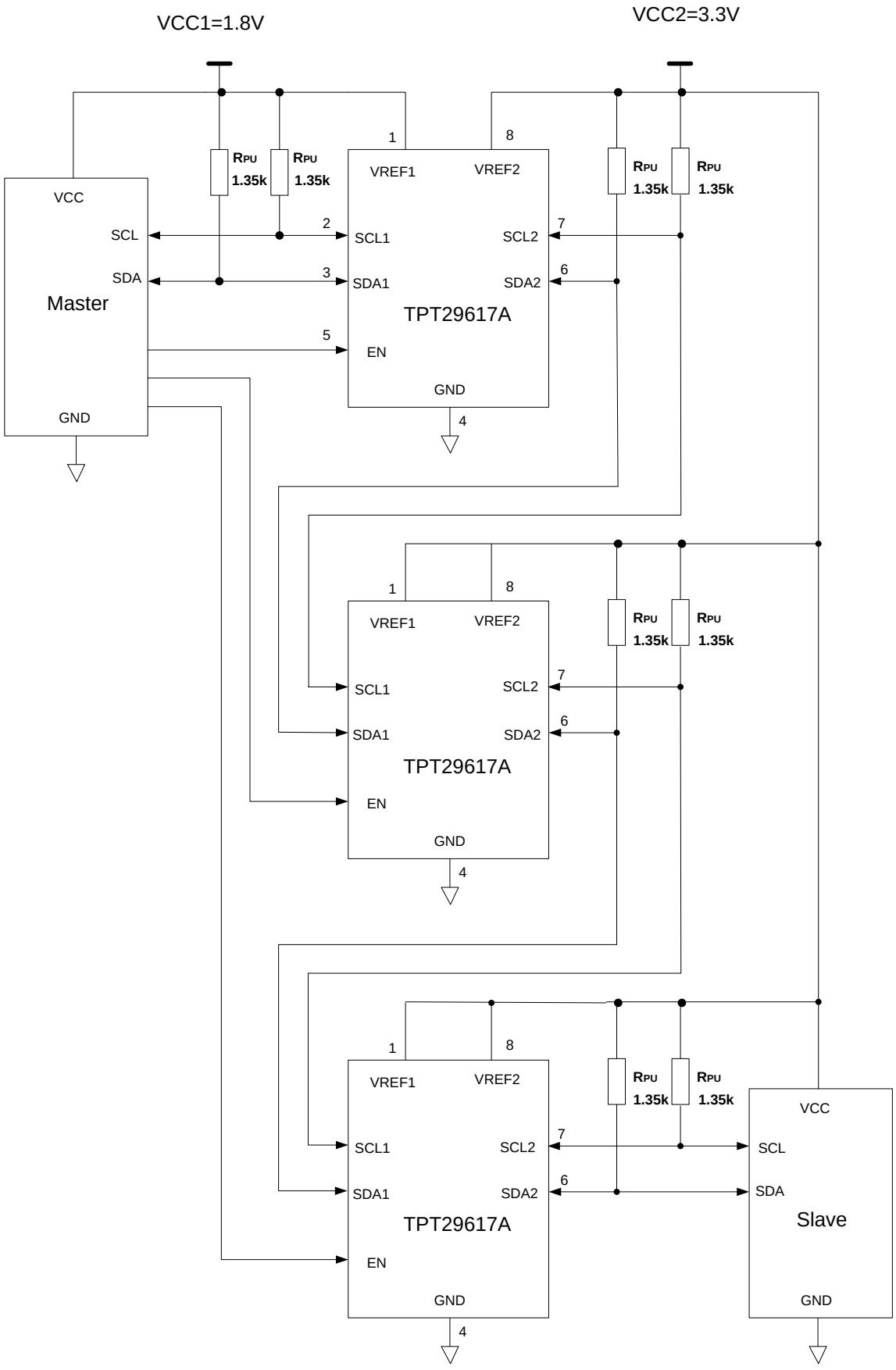
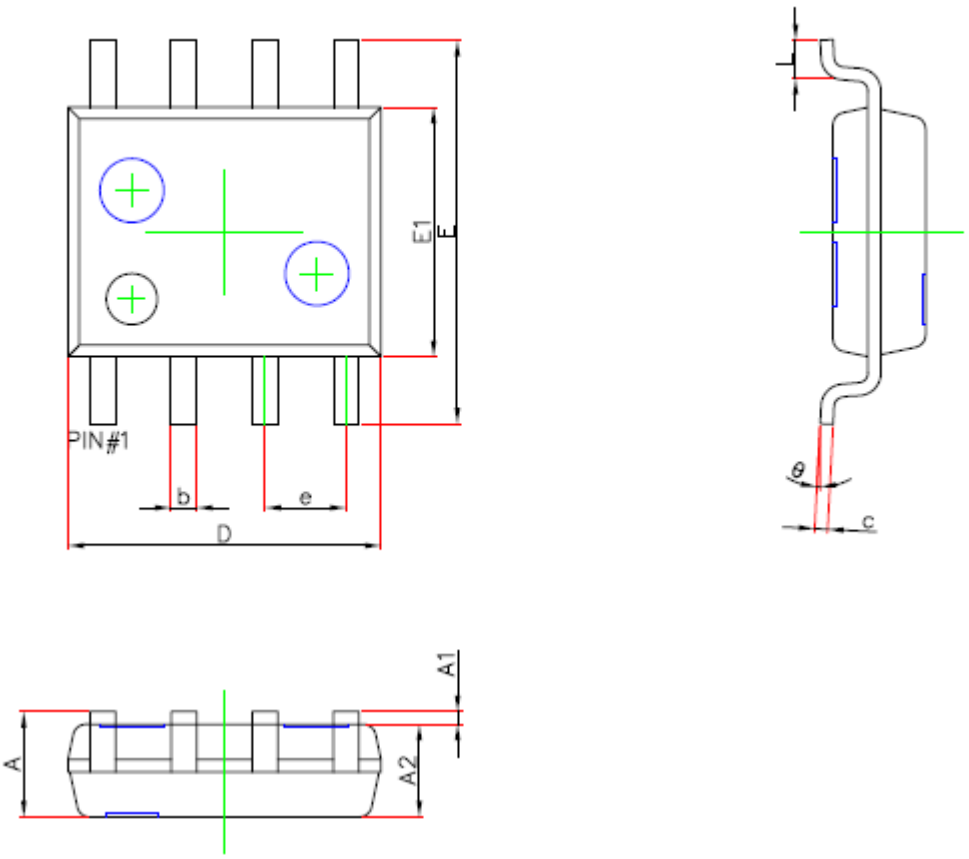


Figure 9. Typical application circuit, series network

Package Outline Dimensions

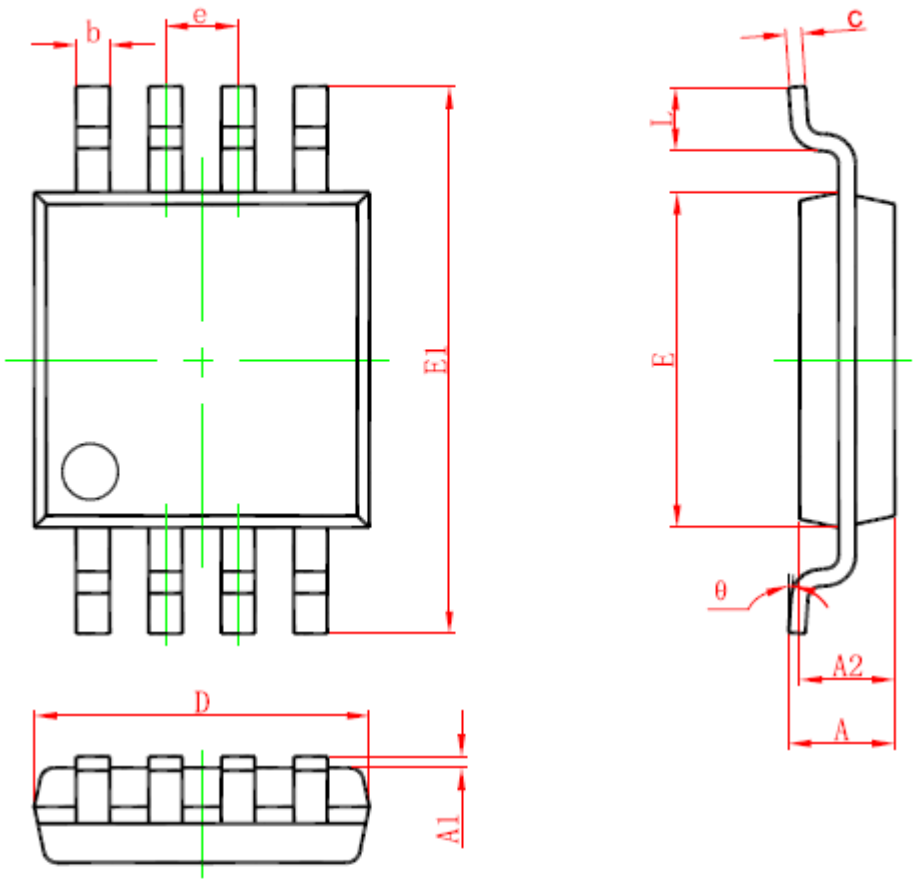
SO1R (SOP8)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270(BSC)		0.050(BSC)	
L	0.400	0.800	0.016	0.031
θ	0°	8°	0°	8°

Package Outline Dimensions

VS1R (MSOP8)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.250	0.380	0.010	0.015
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
e	0.650(BSC)		0.026(BSC)	
E	2.900	3.100	0.114	0.122
E1	4.750	5.050	0.187	0.199
L	0.400	0.800	0.016	0.031
θ	0°	6°	0°	6°