FEATURE

- Analog Input Range
  2 V Full Scale
- 8-Bit Resolution
- Integral Linearity Error
  ±0.5 LSB Max (25°C)
  ±1 LSB Max (–20 °C to 75°C)
- Differential Linearity Error
  ±0.5 LSB Max (25 °C)
  ±0.75 LSB Max (–20 °C to 75 °C)
- Maximum Conversion Rate
  20 Mega-Samples per Second (MSPS) Max
- Built-in clamp function for dc restoration of video signals
- 5-V Single-Supply Operation
- Low Power Consumption
  3PA5510 . . . 127.5 mW Typ
  (includes reference resistor dissipation)
- 3PA5510 is Interchangeable With TI TLC5510

APPLICATIONS

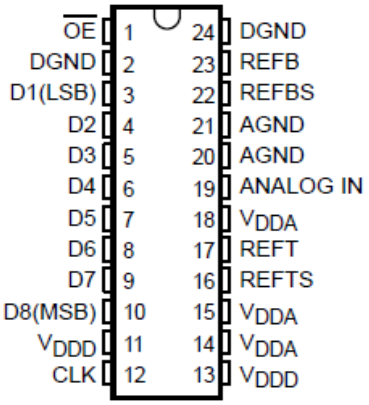
- Digital TV
- Medical Imaging
- Video Conferencing
- High-Speed Data Conversion
- QAM Demodulators

DESCRIPTION

The 3PA5510 is a monolithic, single supply, 8bit, 20 MSPS analog to digital converter with an on chip sample and hold amplifier. The 3PA5510 uses multi-stage differential pipeline architecture at 20 MSPS data rates and guarantees no missing codes over the full operating temperature range. It operates with a single 5-V supply and typically consumes only 130 mW of power. Also included are parallel outputs with high-impedance mode, and internal reference resistors.

The pipeline architecture reduces power consumption and die size compared to flash converters. The latency of the data output valid is 3.5 clocks.

PW OR NS PACKAGE† (TOP VIEW)



† Available in tape and reel only and ordered as the shown in the Available Options table below.

A single clock input is used to control all internal conversion cycles. The digital output data is presented in straight binary output format.

The 3PA5510 uses the three internal reference resistors to create a standard, 2-V, full-scale conversion range using V_{DDA}. No external connection is required to generate the reference voltage. Differential linearity is 0.5 LSB at 25°C and a maximum of 0.75 LSB over the full operating temperature range. Typical dynamic specifications include a differential gain of 1% and differential phase of 0.7 degrees.

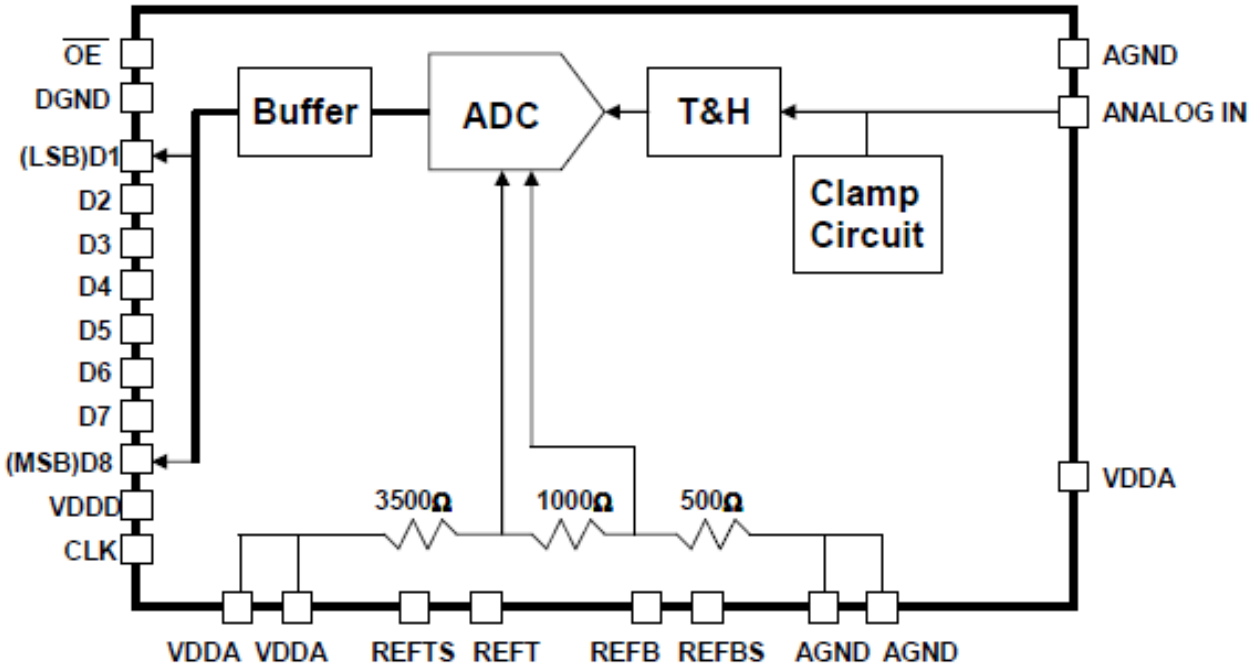
The 3PA5510 is characterized for operation from –20°C to 75°C.

AVAILABLE OPTIONS

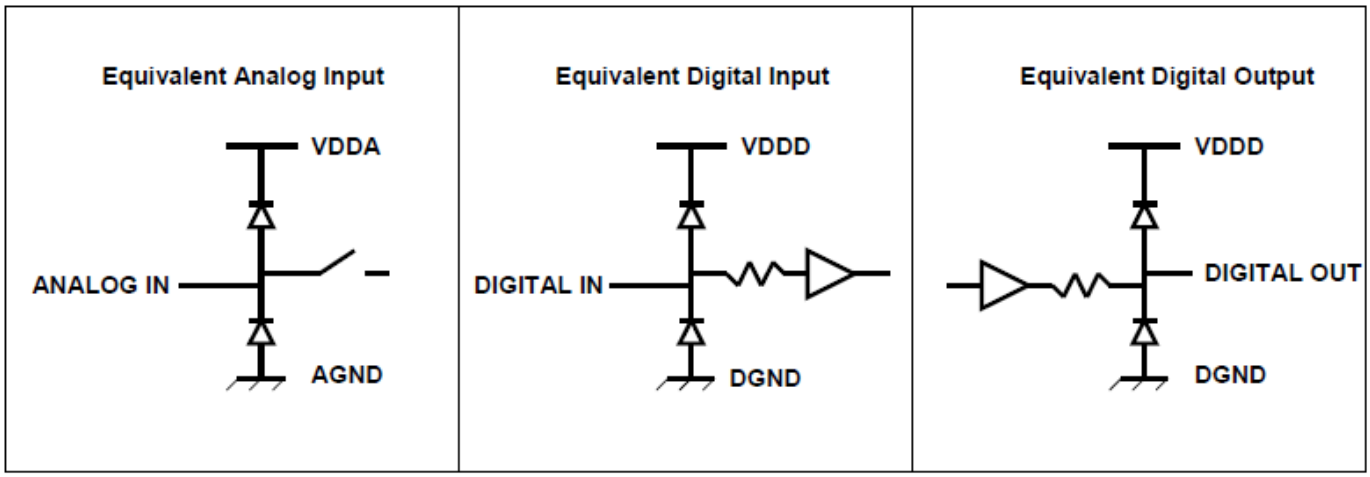
T_A	PACKAGE		MAXIMUM FULL SCALE INPUT VOLTAGE
	TSSOP (PW)	SOP (NS) (TAPE AND REEL ONLY)	
-20°C to 75°C	3PA5510T	3PA5510S	2 V

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of 3Peakic Microelectronics semiconductor products and disclaimers thereto appears at the end of this data sheet.

FUNCTION BLOCK DIAGRAM



SCHEMATICS OF INPUTS AND OUTPUTS



TERMINAL FUNCTION

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AGND	20, 21		Analog ground
ANALOG IN	19	I	Analog input
CLK	12	I	Clock input
DGND	2, 24		Digital ground
D1–D8	3–10	O	Digital data out. D1 = LSB, D8 = MSB
OE	1	I	Output enable. When $\overline{OE}$ = low, data is enabled. When $\overline{OE}$ = high, D1–D8 is in high-impedance state.
VDDA	14, 15, 18		Analog supply voltage
VDDD	11, 13		Digital supply voltage
REFB	23	I	Not used
REFBS	22		Not used
REFT	17	I	Not used
REFTS	16		Not used

ABSOLUTE MAXIMUM RATINGS†

Supply voltage, V_{DDA}, V_{DDD} . . . . . 7 V
Reference voltage input range, V_{REFT}, V_{REFB} . . . . . AGND to V_{DDA}
Analog input voltage range, V_I(ANLG) . . . . . AGND to V_{DDA}
Digital input voltage range, V_I(DGTL) . . . . . DGND to V_{DDD}
Digital output voltage range, V_O(DGTL) . . . . . DGND to V_{DDD}
Operating free-air temperature range, T_A . . . . . –20°C to 75°C
Storage temperature range, T_{stg} . . . . . –55°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply voltage	V_{DDA}–AGND	4.75	5	5.25	V
	V_{DDD}–AGND	4.75	5	5.25	mV
	AGND–DGND	–100	0	100	V
Analog input voltage range, V_I(ANLG)		0		3	V
High-level input voltage, V_{IH}		4			V
Low-level input voltage, V_{IL}				1	V
Pulse duration, clock high, t_w(H) (see Figure 1)		25			ns
Pulse duration, clock low, t_w(L) (see Figure 1)		25			ns

‡The reference voltage levels for the 3PA5510 are derived through an internal resistor divider between V_{DDA} and ground and therefore are not derived from a separate external voltage source (see the electrical characteristics and text).

electrical characteristics at V_{DD} = 5 V, V_{REFT} = 2.5 V, V_{REFB} = 0.5 V, $f_{(CLK)}$ = 20 MHz, TA = 25 C (unless otherwise noted)

DIGITAL I/O

PARAMETER		TEST CONDITIONS†			MIN	TYP	MAX	UNIT
I_{IH}	High-level input current	V_{DD} = MAX,	$V_{IH} = V_{DD}$				5	µA
I_{IL}	Low-level input current	V_{DD} = MAX,	V_{IL} = 0				5	
I_{OH}	High-level output current	$\overline{OE}$ = GND,	V_{DD} = MIN,	$V_{OH} = V_{DD}$–0.5V	–1.5			mA
I_{OL}	Low-level output current	$\overline{OE}$ = GND,	V_{DD} = MIN,	V_{OL} = 0.4 V	2.5			
I_{OZH}	High-level high-impedance-state output leakage current	$\overline{OE} = V_{DD}$,	V_{DD} = MAX	$V_{OH} = V_{DD}$			16	µA
I_{OZL}	Low-level high-impedance-state output leakage current	$\overline{OE} = V_{DD}$,	V_{DD} = MIN	V_{OL} = 0			16	

† Conditions marked MIN or MAX are as stated in recommended operating conditions.

POWER

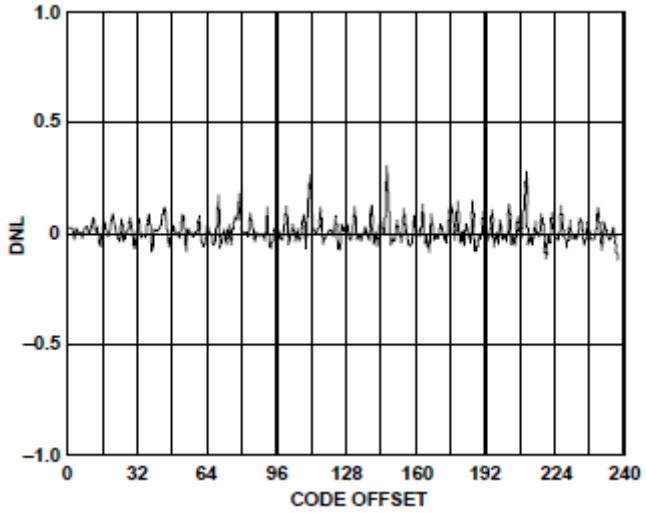
PARAMETER		TEST CONDITIONS†	MIN	TYP	MAX	UNIT
IDD	Supply current	$f_{(CLK)}$ = 20 MHz, National Television System Committee (NTSC) ramp wave input, reference resistor dissipation is separate		25	27	mA
I_{ref}	Reference voltage current	V_{ref} = REFT – REFB = 1 V	0.8	1.0	1.2	mA

† Conditions marked MIN or MAX are as stated in recommended operating conditions.

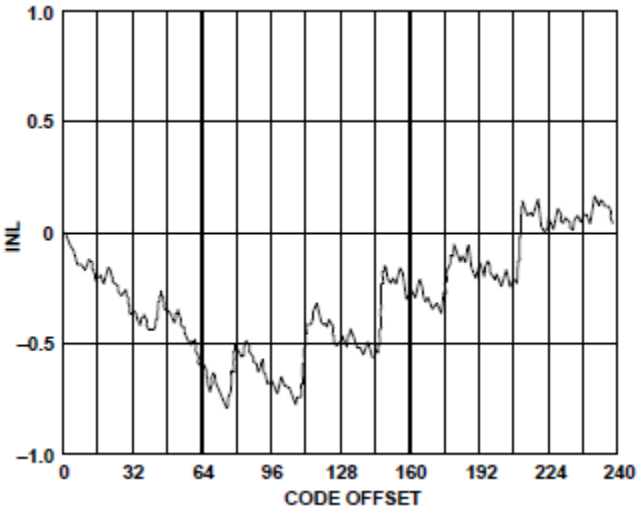
STATIC PERFORMANCE

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
	Self-bias (1), at REFB				0.5		V
	Self-bias (2), REFT – REFB				1.0		
	Self-bias (3), at REFT				1.5		
R_{ref}	Reference voltage resistor	Between REFT and REFB		900	1000	1100	Ω
C_i	Analog input capacitance	V_I(ANLG) = 1 V + 0.07 V_{rms}			2		pF
	Integral nonlinearity (INL)	$f_{(CLK)}$ = 20 MHz,	T_A = 25°C		±0.4	±0.75	LSB
		V_I = 0 V to 2 V	T_A = –20°C to 75°C			±1	
	Differential nonlinearity (DNL)	$f_{(CLK)}$ = 20 MHz,	T_A = 25°C		±0.3	±0.5	
		V_I = 0 V to 2 V	T_A = –20°C to 75°C			±0.75	
E_{ZS}	Zero scale error	Vref = 2*(REFT – REFB) = 2 V		–18	–43	–68	mV
E_{FS}	Full-scale error	Vref = 2*(REFT – REFB) = 2 V		–20	0	20	mV

† Conditions marked MIN or MAX are as stated in recommended operating conditions.



Typical DNL



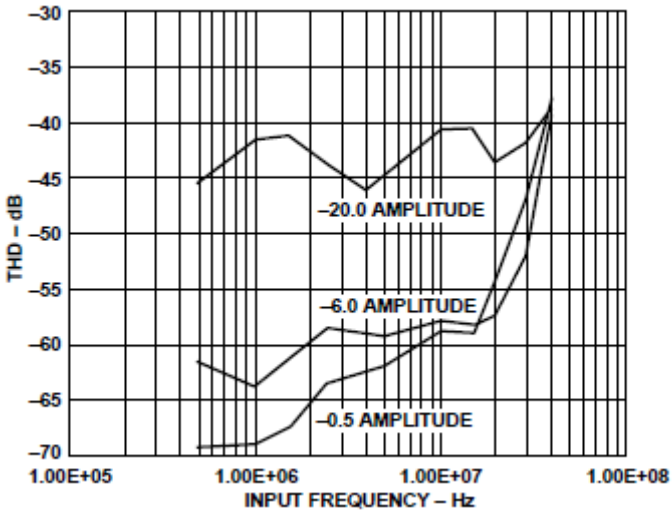
Typical INL

DYNAMIC PERFORMANCE

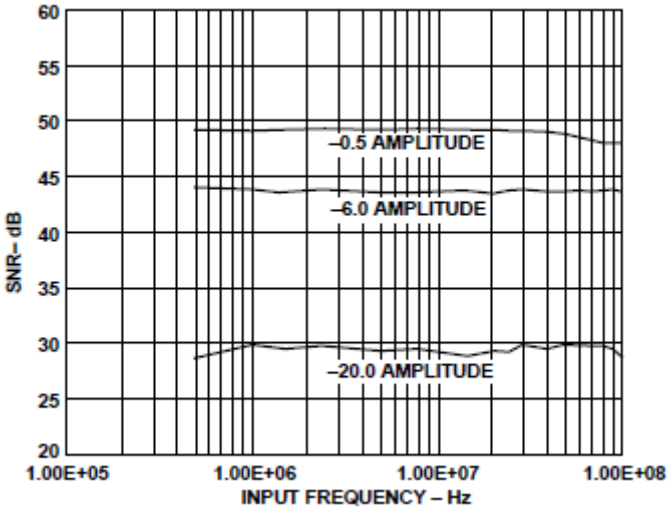
operating characteristics at V_{DD} = 5 V, V_{REFT} = 2.5 V, V_{REFB} = 0.5 V, $f_{(CLK)}$ = 20 MHz, T_A = 25 C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Fconv	Maximum conversion rate	f_I = 1 kHz ramp	$V_{I(ANLG)}$ = 0.5V – 2.5V			20	MSPS
BW	Analog input bandwidth	At – 1 dB			14		MHz
t_d(D)	Digital output delay time	C_L ≤ 10 pF (see Note 1 and Figure 1)			18	30	ns
	Differential gain	NTSC 40 Institute of Radio Engineers (IRE) modulation wave, fconv = 14.3 MSPS			1%		
	Differential phase				0.7		degrees
t_{AJ}	Aperture jitter time				30		ps
t_d(s)	Sampling delay time				4		ns
t_{en}	Enable time, $\overline{OE}\downarrow$ to valid data	C_L = 10 pF			5		ns
t_{dis}	Disable time, $\overline{OE}\uparrow$ to high impedance	C_L = 10 pF			7		ns
	Spurious free dynamic range (SFDR)	Input tone = 1 MHz	T_A = 25°C		45		dB
			Full range		43		
		Input tone = 3 MHz	T_A = 25°C		45		
			Full range		46		
		Input tone = 6 MHz	T_A = 25°C		43		
			Full range		42		
		Input tone = 10 MHz	T_A = 25°C		39		
			Full range		39		
SNR	Signal to noise ratio	T_A = 25 °C			46		dB
		Full range			44		

NOTE 1: C_L includes probe and jig capacitance.



THD vs. Input Frequency



SNR vs. Input Frequency

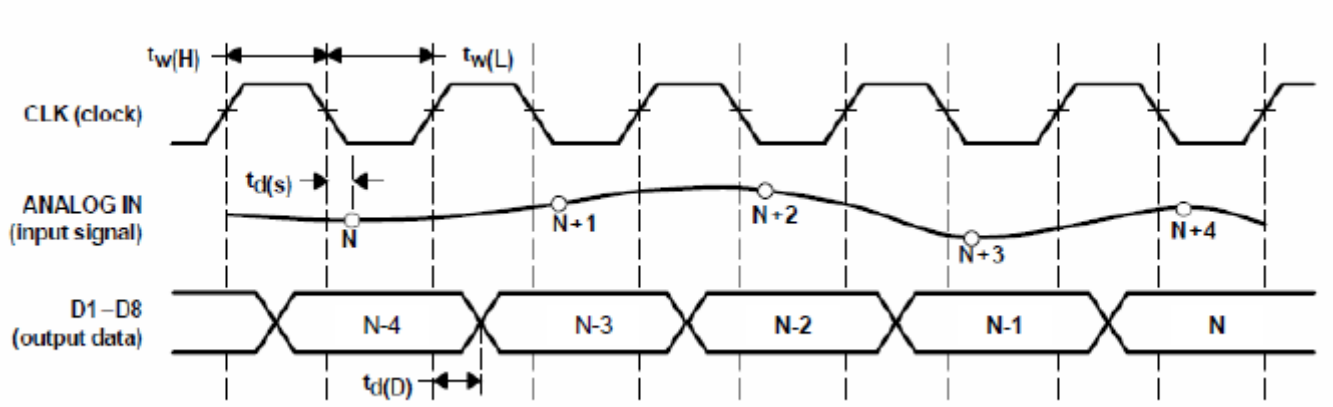


Figure 1. I/O Timing Diagram

PRINCIPLES OF OPERATION

FUNCTIONAL DESCRIPTION

The 3PA5510 implements a pipelined multistage architecture to achieve high sample rate with low power. The 3PA5510 distributes the conversion over several smaller A/D sub-blocks, refining the conversion with progressively higher accuracy as it passes the results from stage to stage. As a consequence of the distributed conversion, the 3PA5510 requires a small fraction of the 256 comparators used in a traditional flash type A/D. A sample and hold function within each of the stages permits the first stage to operate on a new input sample while the second, third and fourth stages operate on the three preceding samples

INTERNAL REFERENCING

The three internal resistors shown with V_{DDA} can generate a 2-V reference voltage. These resistors are integrated internally. No external connection is necessary.

To generate internal reference voltage the resistors are connected as shown in Figure 3.This connection provides the 1-V differential reference voltage (REFT-REFB). Because of the fully differential ADC architecture of 3PA5510, this provides the standard video 2-V reference for the nominal digital output.

The REFTS, REFT, REFBS, and REFB pins are not used and can be either left floating or connected to any capacitors.

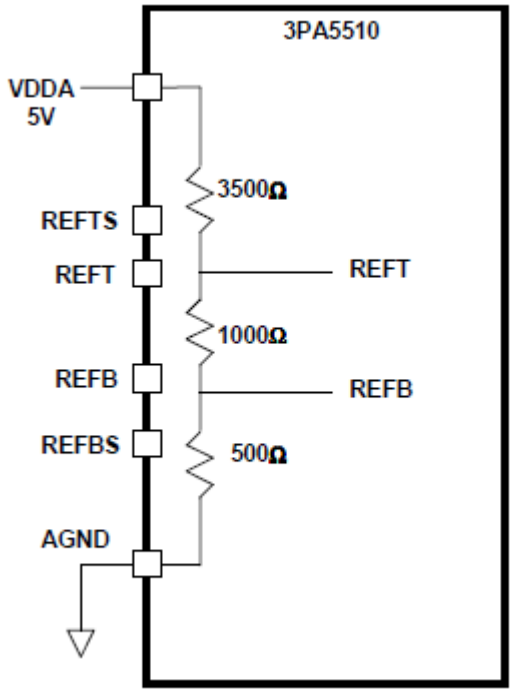


Figure 3. No External Connection necessary for a 2-V Analog Input Span Using the Internal-Reference Resistor Divider

PRINCIPLES OF OPERATION

FUNCTIONAL OPERATION

The output code change with input voltage is shown in Table 1.

TABLE 1. FUNCTIONAL OPERATION

INPUT SIGNAL VOLTAGE	STEP	DIGITAL OUTPUT CODE							
		MSB							LSB
2*(REFT-REFB)	255	0	0	0	0	0	0	0	0
	•								
•	•	•	•	•	•	•	•	•	•
•	128	0	1	1	1	1	1	1	1
•	127	1	0	0	0	0	0	0	0
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
O	0	1	1	1	1	1	1	1	1

APPLICATION INFORMATION

The following notes are design recommendations that should be used with the device.

- External analog and digital circuitry should be physically separated and shielded as much as possible to reduce system noise.
- RF breadboarding or printed-circuit-board (PCB) techniques should be used throughout the evaluation and production process. Breadboards should be copper clad for bench evaluation.
- Since AGND and DGND are connected internally, the ground lead in must be kept as noise free as possible. A good method to use is twisted-pair cables for the supply lines to minimize noise pickup. An analog and digital ground plane should be used on PCB layouts when additional logic devices are used. The AGND and DGND terminals of the device should be tied to the analog ground plane.
- V_{DDA} to AGND and V_{DDD} to DGND should be decoupled with 1-μF and 0.01-μF capacitors, respectively, and placed as close as possible to the affected device terminals. A ceramic-chip capacitor is recommended for the 0.01-μF capacitor. Care should be exercised to ensure a solid noise-free ground connection for the analog and digital ground terminals.
- V_{DDA}, AGND, and ANALOG IN should be shielded from the higher frequency terminals, CLK and D0–D7. When possible, AGND traces should be placed on both sides of the ANALOG IN traces on the PCB for shielding.
- In testing or application of the device, the resistance of the driving source connected to the analog input should be 10 Ω or less within the analog frequency range of interest.

APPLICATION INFORMATION

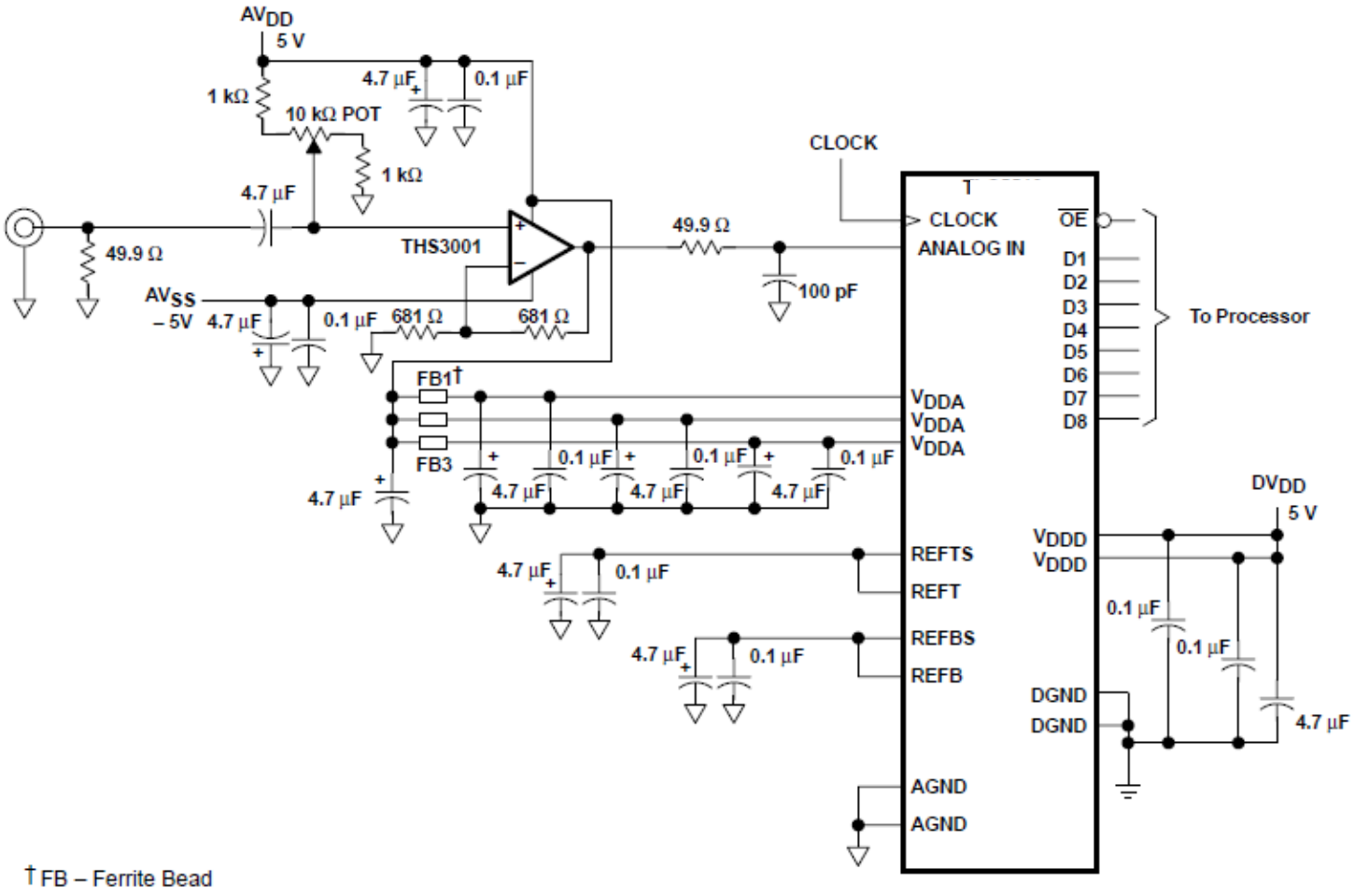
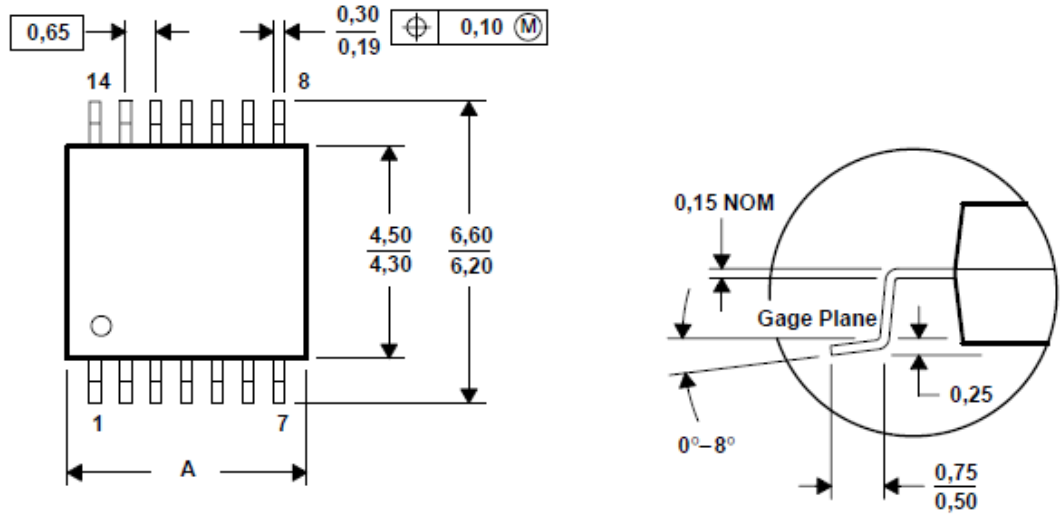


Figure 7. 3PA5510 Application Schematic

MECHANICAL DATA

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



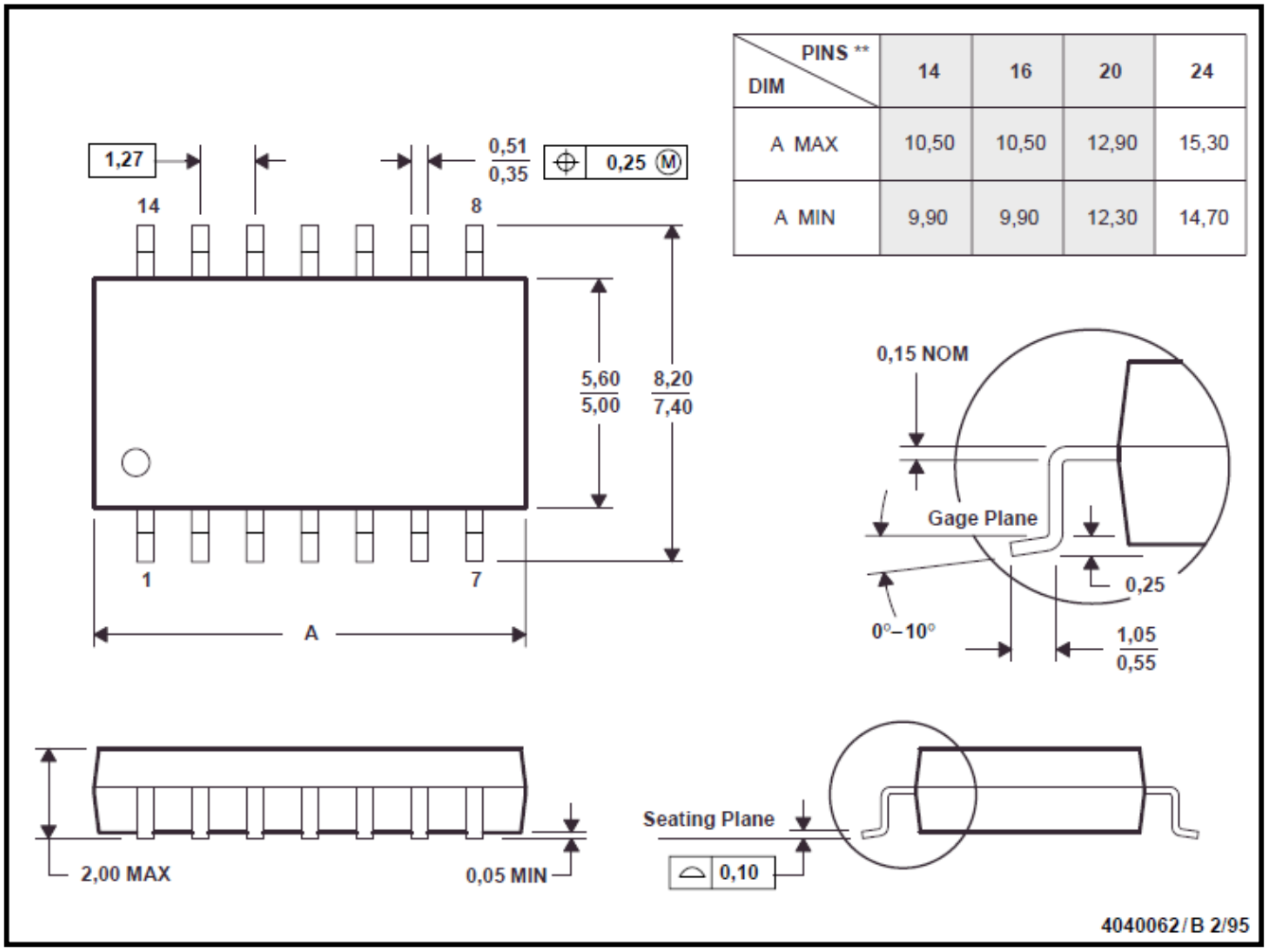
DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



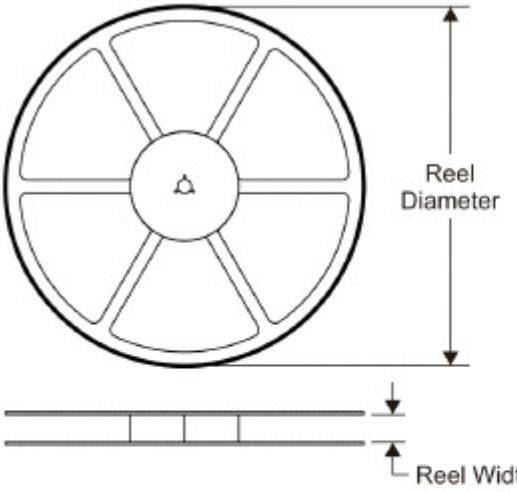
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PACKAGING INFORMATION

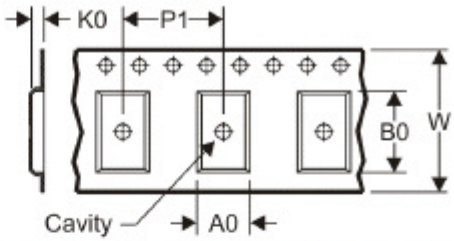
Orderable Device	Package Type	Pins	Package Qty
3PA5510SR	SO	24	2000
3PA5510T	TSSOP	24	60
3PA5510TR	TSSOP	24	2000

TAPE AND REEL INFORMATION

REEL DIMENSIONS

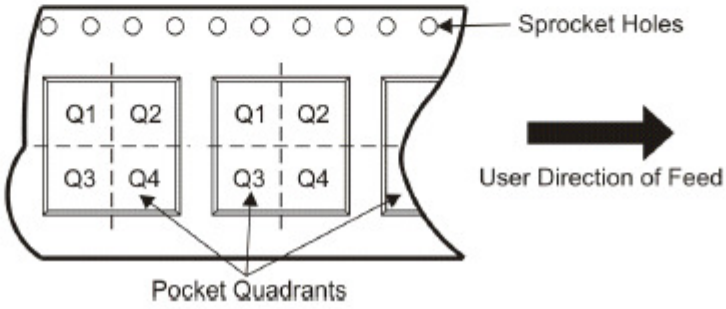


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

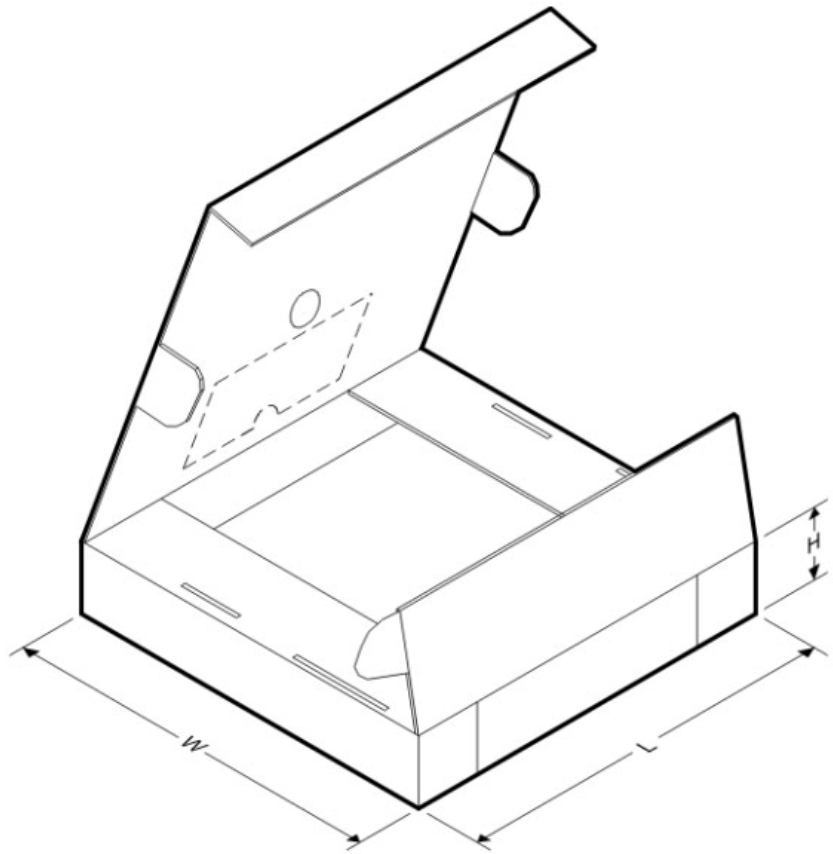
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



***All dimensions are nominal**

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
3PA5510SR	SO	NS	24	2000	330.0	24.4	8.2	15.4	2.5	12.0	24.0	Q1
3PA5510TR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

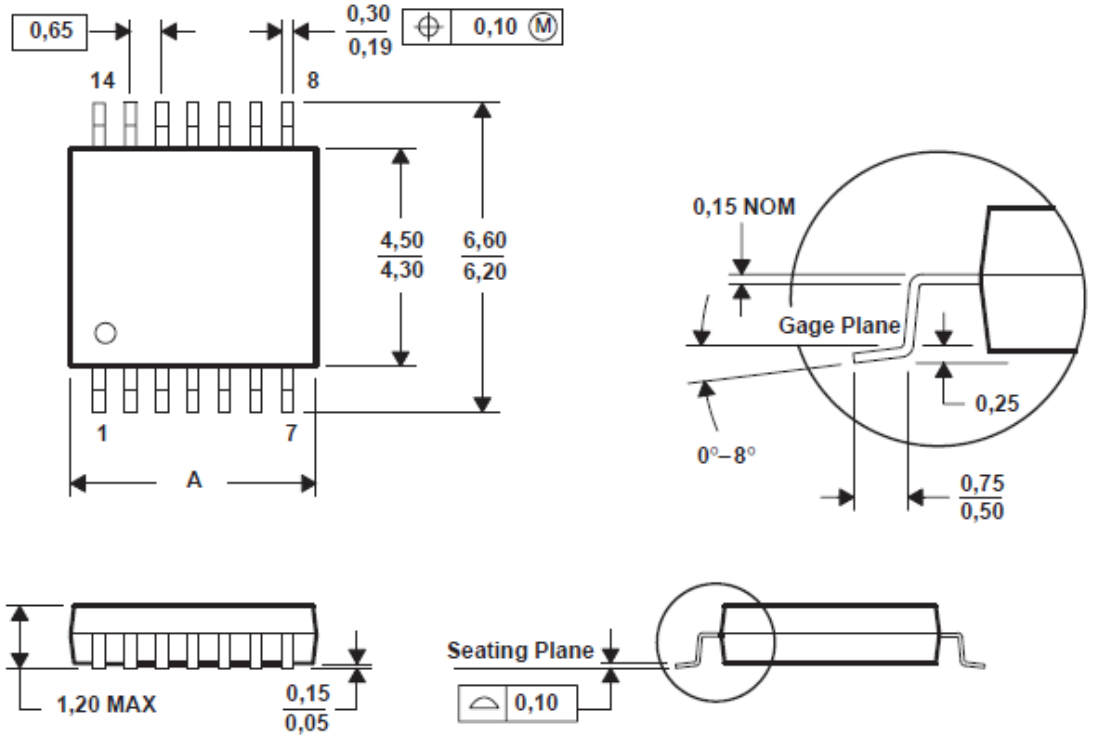


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
3PA5510SR	SO	NS	24	2000	346.0	346.0	41.0
3PA5510TR	TSSOP	PW	24	2000	346.0	346.0	33.0

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

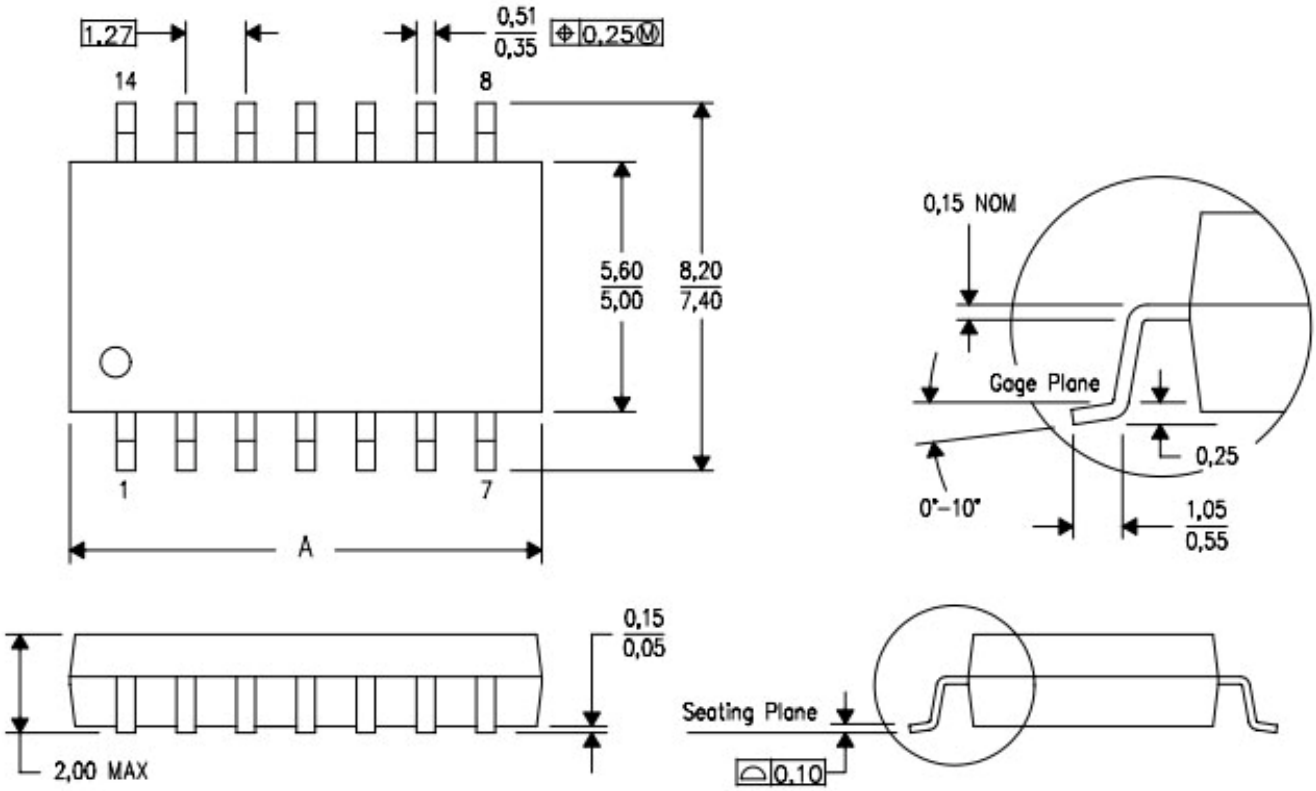
NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153

MECHANICAL DATA



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notics.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.15.

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